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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,671	07/28/2004	Chih-Wei Hung	13085-US-PA	4670

31561 7590 01/06/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/710,671	HUNG ET AL.	
	Examiner	Art Unit	
	William Kraig	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The previous objection to the Drawings is withdrawn in view of the Applicant's amended replacement drawing sheet, which was submitted on 11/24/05.

Specification

2. The previous objections to the specification are withdrawn in view of the Applicant's amendment to the specification, which was submitted on 11/24/05.

Claim Objections

3. The previous objection to claim 1 is withdrawn in view of the Applicant's amendment to the claims, which was submitted on 11/24/05.

Claim Rejections - 35 USC § 112

4. The previous rejections under 35 U.S.C. 112 are withdrawn in view of the Applicant's amendments to the claims, which were submitted on 11/24/05.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh (U.S. Patent # 6645813).

Regarding claim 1, Fig. 2h of Hsieh discloses a non-volatile memory structure, comprising:

a substrate(100);

a plurality of gate structures(multiple layered structures built on top of oxide layers 110) disposed on the substrate(100), wherein each gate structure(multiple layered structures built on top of oxide layers 110) comprises, from the substrate(100), at least a bottom dielectric layer(bottom oxide layer of 130(Hsieh, Col. 7, Lines 14-20)), a charge-trapping layer(Nitride layer of 130(Hsieh, Col. 7, Lines 14-20)) , an upper dielectric layer(upper oxide layer of 130(Hsieh, Col. 7, Lines 14-20)), a control gate(140) and a cap layer(150) (Hsieh, Col. 7, Lines 34-37).

a plurality of select gate structures(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)), wherein each of the select gate structures(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)) is disposed on one side of each gate structure(multiple layered structures built on top of oxide layers 110) respectively such that the gate structures(multiple layered structures built on top of oxide layers 110) are serially connected together to form a memory cell row(the multi-bit split-gate flash memory cell described by Hsieh in Col. 8, Lines 36-52 and shown in Fig. 5f), wherein each select gate structure(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)) comprises, from the substrate(100), at least a select gate dielectric layer(210) and a select gate(220(divided as described on Lines 26-40, Column 8 of Hsieh));

a plurality of spacers(170), disposed between the gate structures(multiple layered structures built on top of oxide layers 110) and the select gate structures(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)); and

a source/drain region(107), disposed in the substrate(100) on each side of the memory cell row(the multi-bit split-gate flash memory cell described by Hsieh in Col. 8, Lines 36-52 and shown in Fig. 5f).

Regarding claim 2, Hsieh discloses the non-volatile memory structure of claim 1, wherein said spacers(170) are formed adjacent to and on both sides of each gate structure(multiple layered structures built on top of oxide layers 110)(Fig. 5f), wherein

there are spaces(Fig. 5e, (125)) between said spacers(170) not occupied by said gate structures(multiple layered structures built on top of oxide layers 110), wherein each of the select gate structures(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)) completely fills said spaces(Fig. 5e, (125)) between said spacers(170).

Regarding claim 3, Hsieh discloses the non-volatile memory structure of claim 1, wherein material constituting the charge-trapping layer comprises silicon nitride. (Hsieh, Col. 7, Lines 14-20)

Regarding claim 4, Hsieh discloses the non-volatile memory structure of claim 1, wherein material constituting the bottom dielectric layer(bottom oxide layer of 130(Hsieh, Col. 7, Lines 14-20)) and the upper dielectric layer(upper oxide layer of 130(Hsieh, Col. 7, Lines 14-20)) comprises silicon oxide. (Hsieh, Col. 7, Lines 14-20)

Regarding claim 5, Hsieh discloses the non-volatile memory structure of claim 1, wherein material constituting the control gate(140) and the select gate (220(divided as described on Lines 26-40, Column 8 of Hsieh)) comprises polysilicon. (Hsieh, Col. 7, Lines 22-24)(Hsieh, Col. 8, Lines 26-40)

Regarding claim 6, Hsieh discloses the semiconductor device of claim 1 wherein the select gate dielectric layer has a thickness between about 160 Angstroms and 170 Angstroms. (Hsieh, Col. 8, Lines 20-26)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-10 and 19-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh.

Regarding claim 7, Hsieh discloses a non-volatile memory structure, comprising:

a gate structure (multiple layered structure built on top of oxide layers 110) having at least a bottom dielectric layer (bottom oxide layer of 130(Hsieh, Col. 7, Lines 14-20)), a charge trapping layer (Nitride layer of 130(Hsieh, Col. 7, Lines 14-20)), an upper dielectric layer (upper oxide layer of 130(Hsieh, Col. 7, Lines 14-20)), a control gate (140) and a cap layer (150) (Hsieh, Col. 7, Lines 34-37) over a substrate (100);

a select gate (220), disposed on one side of the gate structure (multiple layered structure built on top of oxide layers 110);

a spacer (170), disposed between the gate structure (multiple layered structure built on top of oxide layers 110) and the select gate (220);

a select gate dielectric layer (210), disposed between the select gate (220) and the substrate (100);

a source region (107), disposed in the substrate (100) on one side of the gate structure (multiple layered structure built on top of oxide layers (110)) opposite from the select gate (16); and

a drain region (109), disposed in the substrate (100) adjacent to the select gate (220).

Hsieh, however, fails to teach the thickness of the bottom dielectric layer being between about 20 and 30 Angstroms.

It would have been obvious to one of ordinary skill in the art to decrease the thickness of the bottom dielectric layer in the device of Hsieh. The claim to a decrease in the thickness of the bottom dielectric layer constitutes an optimization of ranges. *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996)

Regarding claim 8, Hsieh discloses the non-volatile memory structure of claim 7, wherein material constituting the charge-trapping (memory) layer comprises silicon nitride. (Hsieh, Col. 7, Lines 14-20)

Regarding claim 9, Hsieh discloses the non-volatile memory structure of claim 7, wherein material constituting the bottom dielectric layer (bottom oxide layer of 130(Hsieh, Col. 7, Lines 14-20)) comprises silicon oxide. (Hsieh, Col. 7, Lines 14-20)

Regarding claim 10, Hsieh discloses the non-volatile memory structure of claim 7, wherein material constituting the upper dielectric layer (upper oxide layer of 130 (Hsieh, Col. 7, Lines 14-20)) comprises silicon oxide. (Hsieh, Col. 7, Lines 14-20)

Regarding claim 19, Hsieh discloses the structure of claim 1, wherein material constituting the cap layer comprises silicon nitride.

Paragraph 37 of Abedifard (U.S. Patent Publication 2002/0074592) teaches that a silicon oxide cap layer and a silicon nitride cap layer may be used interchangeably. Abedifard thus serves as evidence that it was known in the art at the time the invention was made that silicon oxide and silicon nitride could both be used as cap layers. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute a silicon oxide cap layer for the silicon nitride cap layer of Hsieh. *Smith v. Hayashi*, 209 USPQ 754 (Bd. of Pat. Inter. 1980)

Regarding claim 20, Hsieh discloses the structure of claim 7, but fails to teach the thickness of the charge trapping layer being between about 30 and 50 Angstroms.

It would have been obvious to one of ordinary skill in the art to decrease the thickness of the charge trapping layer in the device of Hsieh. The claim to a decrease in the thickness of the charge trapping layer constitutes an optimization of ranges. *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996)

Regarding claim 21, Hsieh discloses the structure of claim 7, wherein the upper dielectric layer has a thickness between about 20 and 40 Angstroms. (Hsieh, Col. 7, Lines 19-21)

Regarding claim 22, Hsieh discloses the semiconductor device of claim 7 wherein the select gate dielectric layer has a thickness between about 160 Angstroms and 170 Angstroms. (Hsieh, Col. 8, Lines 20-26)

Double Patenting

6. The Examiner's previous assertion that claim 8 would be objected to as being a substantially duplicate claim if claim 3 were to be found allowable is withdrawn in view of the Applicant's amendment to the claims, dated 11/24/05.

Response to Arguments

Applicant's arguments filed 11/24/05 have been fully considered but they are not persuasive.

Applicant first argues, regarding claim 1, that Hsieh teaches a device that is different from the instant invention for the reasons that "Hsieh's silicon nitride layer is embedded within the ONO film, which is located between the floating gate (FG) and the control gate (CG)" while the instant invention "teaches a charge trapping layer made from silicon nitride to be placed between the upper dielectric layer and bottom dielectric layers, essentially replacing the FGs in prior art and in Hsieh". Examiner points out that

an ONO layer, by definition, is formed of three layers: a bottom oxide layer, a middle nitride layer, and an upper oxide layer (see Hsieh, Col. 7, Lines 15-20). Thus, the ONO layer of Hsieh is an express teaching of a charge trapping layer made from silicon nitride to be placed between an upper dielectric layer and a bottom dielectric layer, as argued by the Applicant. The existence and location of the floating gate in Hsieh is irrelevant, as Hsieh discloses all limitations of the claimed invention, as outlined in the above rejection.

Applicant also argues, regarding claim 1, that "Hsieh's FG is made out of polysilicon while the present invention teaches a charge trapping layer" and thus "a person of ordinary skill in the art would not depart from Hsieh's teaching and replace the polysilicon FG with a silicon nitride layer." Examiner argues that it is not necessary to "replace" the polysilicon floating gate of Hsieh with a silicon nitride layer in order for Hsieh's disclosed invention to read on the limitations of the claimed instant invention, as outlined in the rejection above.

Applicant finally argues, regarding claim 1, that Hsieh's teaching that "the fourth polysilicon layer…serves as the word line that is oriented perpendicular to the first and second bit lines" departs from the instant invention's teaching that the CG line serves as the word line and the control gate line is aligned parallel to the SG lines. In response to this argument, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's arguments with respect to claim 7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFK

GEORGE ECKERT
PRIMARY EXAMINER